AMENDMENTS TO THE CLAIMS

Claims 1-5 (Canceled)

6. (Previously Presented) The semiconductor device according to claim 27, wherein said antireflection layer includes a first antireflection layer extending in a direction of a length of said fuse, and a second antireflection layer extending in a direction traversing the first antireflection layer.

7. (Cancelled)

8. (Previously Presented) The semiconductor device according to claim 28, wherein said reflection layer includes a dummy metal line provided between said fuses in a planar view and a transparent resin film covering the dummy metal line, said transparent resin film forming a recessed and protruded surface having a portion overlying the dummy metal line and projecting closer to said fuse than a portion between the dummy metal lines.

9. (Previously Presented) The semiconductor device according to claim 26, wherein said fuse is formed from at least two portions different in width.

Claims 10-11 (Cancelled)

12. (Previously Presented) The semiconductor device according to claim 26, wherein an oxidation speed of the metal forming said fuse is faster than an oxidation speed of the metal forming the connection portion of said interconnection line.

13. (Previously Presented) The semiconductor device according to claim 26, wherein said fuse is formed of a copper metal, and

the connection portion of said interconnection line is formed of an aluminum metal.

Claims 14-16 (Canceled)

17. (Withdrawn) A method of manufacturing a semiconductor device, the method comprising:

forming a circuit structure with an interconnection line, the interconnection line having a connection portion, on a substrate;

electrically connecting a fuse to the connection portion of the interconnection line, the fuse and the connection portion being formed of different metals; and

selectively blowing the fuse when the circuit structure is to be changed.

18. (Withdrawn) The method according to claim 17, comprising forming the fuse of a metal having an oxidation speed faster than an oxidation speed of the metal forming the connection portion.

19. (Withdrawn) The method according to claim 17, comprising:

forming the fuse of a copper metal; and

forming the connection portion of an aluminum metal.

20 (Withdrawn) The method according to claim 19, comprising forming the copper metal fuse by a damascene process followed by chemical mechanical polishing.

21. (Withdrawn) The method according to claim 1, comprising:

forming the interconnection line as a multilayer interconnection line;

providing the fuse at a same layer as one layer of the multilayer interconnection line; and

providing an antireflection layer closer to the substrate than is a layer of the fuse.

22. (Withdrawn) The method according to claim 21, wherein the antireflection layer includes a first antireflection layer extending in the direction of a length of the fuse and a second antireflection layer extending in a direction traversing the first antireflection layer.

23. (Withdrawn) The method according to claim 1, comprising:

forming the interconnection line as a multilayer interconnection line;

providing the fuse at a same layer as one layer of the multilayer interconnection line; and

providing a reflection layer closer to the substrate than is a layer of the fuse.

24. (Withdrawn) The method according to claim 22, comprising:

forming a plurality of fuses; and

forming the reflection layer with a dummy metal line provided between the fuses in a planar view and a transparent resin film covering the dummy metal line, the transparent metal film forming a recessed and protruded surface having a portion overlying the dummy metal line and projecting closer to the fuse than a portion between the dummy metal lines.

25. (Withdrawn) The method according to claim 17, comprising providing a fuse with at least two portions having different widths.

26. (Currently Amended) A semiconductor device formed on a substrate, comprising:

an interconnection line formed on said substrate and provided to structure a prescribed circuit; [[and]]

a fuse incorporated into said interconnection line[[,]]; and

a passivation film covering said fuse, said passivation film having a flat surface, wherein

said fuse and a connection portion of said interconnection line electrically connected to the fuse being formed of different metals, ~~wherein~~ and

said fuse is formed of [[the]] a copper metal formed in a damascene process and planarized by a CMP (Chemical Mechanical Polishing) process.

27. (Previously Presented) A semiconductor device formed on a substrate, comprising:

an interconnection line formed on said substrate and provided to structure a prescribed circuit; and

a fuse incorporated into said interconnection line,

said fuse and a connection portion of said interconnection line electrically connected to the fuse being formed of different metals, wherein

said interconnection line is formed as a multilayer interconnection line,

said fuse is provided at a same layer as one layer of the multilayer interconnection line, and

an antireflection layer is provided closer to said substrate than is a layer of said fuse.

28. (Previously presented) A semiconductor device formed on a substrate, comprising:

an interconnection line formed on said substrate and provided to structure a prescribed circuit; and

a fuse incorporated into said interconnection line,

said fuse and a connection portion of said interconnection line electrically connected to the fuse being formed of different metals, wherein

said interconnection line is formed as a multilayer interconnection line,

said fuse is provided at a same layer as one layer of the multilayer interconnection line, and

a reflection layer is provided closer to said substrate than is a layer of said fuse.